

1 What is claimed is:

2
3 **1.** A method for determining a plurality of clock delay values, each delay value associated
4 with a delay element on a clock line leading to a clock sink in a synchronous circuit, the
5 method comprising:

6 determining an initial set of delay values; and

7 executing an optimization algorithm, beginning with the initial set of delay values,
8 to arrive at a set of delay values that at least approximately meet a criteria while satisfying
9 timing constraints associated with selected pairs of logically connected clock sinks,
10 wherein the optimization algorithm comprises randomly modifying the set of delay values.

11
12 **2.** The method of claim 1 wherein the determining step comprises:

13 randomly selecting the initial set of delay values.

14
15 **3.** The method of claim 1 wherein the determining step comprises:

16 executing a linear programming algorithm to determine the initial set of delay
17 values.

18
19 **4.** The method of claim 1 wherein the determining step comprises:

20 executing a quadratic programming algorithm to determine the initial set of delay
21 values.

22
23 **5.** The method of claim 1 wherein the optimization algorithm is a genetic algorithm.

24
25 **6.** The method of claim 5 wherein determining step comprises:

26 determining multiple initial sets of delay values;

27
28 **7.** The method of claim 5 wherein the genetic algorithm comprises the following steps:

29 selecting parent sets of delay values;

30 crossing over so as to produce a child set of delay values;

1 mutating the child set of delay values;
2 evaluating how well the child set of delay values meets the criteria; and
3 conditionally discarding the child set on the basis of the evaluating step.
4

5 **8.** The method of claim 7 wherein the selecting step comprises:

6 conducting a random tournament.
7

8 **9.** The method of claim 7 wherein the crossing over step comprises:

9 dividing two parents into corresponding regions, wherein the number and locations
10 of the regions are random; and

11 randomly swapping corresponding regions of the parents, so as to result in two
12 region-by-region swapped set of delay values that are children.
13

14 **10.** The method of claim 7 wherein the mutating step comprises:

15 adding to each delay value in the child set of delay values a Gaussian random
16 variable having zero mean and a predetermined variance.
17

18 **11.** The method of claim 7 wherein the evaluating step comprises:

19 calculating an objective function for the child set; and
20 determining whether the child set satisfies the timing constraints.
21

22 **12.** The method of claim 7 further comprising:

23 iteratively repeating the selecting, crossing over, mutating, evaluating and
24 conditionally discarding steps.
25

26 **13.** The method of claim 1 wherein the optimization algorithm is a gradient search
27 algorithm.
28

29 **14.** The method of claim 13 wherein the gradient descent algorithm comprises the
30 following steps:

1 perturbing a set of delay values;
2 evaluating how well the perturbed set of delay values meets the criteria; and
3 conditionally discarding the perturbed set on the basis of the evaluating step.

- 4
5 **15.** The method of claim 14 further comprising:
6 iteratively repeating the perturbing, evaluating and conditionally discarding steps;
7 and
8 if the perturbed set is not discarded, then adjusting the values of the perturbed set
9 in the same direction relative to the corresponding values in the initial set.

- 10
11 **16.** The method of claim 14 wherein the perturbing step comprises
12 randomly perturbing the initial set of values.

- 13
14 **17.** The method of claim 1 wherein the timing constraints are defined substantially as
15 follows:

$$16 \quad T_S + C_i + G_i + D_{ijL} < T_{CLK+} + C_j + G_j$$

$$17 \quad C_i + G_i + D_{ijs} > C_j + G_j + T_H$$

18 where T_S is the setup time, T_H is the hold time, D_{ijL} is the longest propagation delay between a
19 pair of logically connected clock sinks i and j , D_{ijs} is the shortest propagation delay between a
20 pair of logically connected clock sinks i and j , C_i and C_j measure relative clock skew between
21 the sinks i and j , and G_i and G_j are the delay values for the sinks i and j out of the set of delay
22 values.

- 23
24 **18.** The method of claim 17 wherein the criteria is minimization of a quantity selected
25 from the group consisting of a quantity related to a clock frequency, a quantity related to a
26 sum of the set of delay values, and a quantity related to the distances of the delay values
27 from a target.

1 **19.** A synchronous circuit comprising:

2 a plurality of clock sinks;

3 a plurality of clock delay elements connected to the clock sinks, each clock delay
4 element having a delay value, wherein the delay values are set according to a method
5 comprising a step of determining initial values for the delay values and a step of executing
6 an optimization algorithm, beginning with the initial set of delay values, to arrive at a set
7 of delay values that at least approximately meet a criteria while satisfying timing
8 constraints associated with selected pairs of logically connected clock sinks, wherein the
9 optimization algorithm comprises randomly modifying the set of delay values.

10
11 **20.** A computer readable medium on which is embedded computer software, the software
12 comprising a program, the program performing a method for determining a plurality of
13 clock delay values, each delay value associated with a delay element on a clock line
14 leading to a clock sink in a synchronous circuit, the method comprising:

15 determining an initial set of delay values; and

16 executing an optimization algorithm, beginning with the initial set of delay values,
17 to arrive at a set of delay values that at least approximately meet a criteria while satisfying
18 timing constraints associated with selected pairs of logically connected clock sinks,
19 wherein the optimization algorithm comprises randomly modifying the set of delay values.